

Sub. D. ~~a heavily doped region of buried layer having the second conductivity type formed between the first contact region in the first well and an interface between a surface of the first well and opposite from the first contact region within the semiconductor substrate.~~

Q1 2. (Currently Amended) The semiconductor device as claimed in claim 1, further comprising:

a second well having the first conductivity type formed in a second region in the major surface of the semiconductor substrate;

a second MOS transistor having the second conductivity type and a second contact region having the second conductivity type formed in the second well; and

a heavily doped region of buried layer having the first conductivity type formed between the second contact region in the second well and a surface of an interface between the second well on an opposite portion of the second well from the second contact region within and the semiconductor substrate.

Q2 Sub. D. 3. (Previously Amended) The semiconductor device as claimed in claim 2, wherein the junction depth of the first and second wells is 1.5 to 2.0 μm .

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4. (Previously Amended) The semiconductor device as claimed in claim 2, wherein the concentration of the heavily doped region of buried layer having the first conductivity type is higher than that of the second well and lower than that of the second contact region.

5. (Previously Amended) The semiconductor device as claimed in claim 2, wherein the concentration of the heavily doped region of buried layer having the second conductivity type is higher than that of the first well and lower than that of the first contact region.

6. (Canceled)

7. (Canceled)

8. (Canceled)

9. (Canceled)

10. (Canceled)

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~~11. (Currently Amended) The semiconductor device as claimed in claim 2 1, wherein the heavily doped region having the first second conductivity type is separated from the first contact region does not extend under the second MOS transistor in the second well.~~

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~~12. (Previously Added) The semiconductor device as claimed in claim 1, wherein the heavily doped region of the second conductivity type does not extend under the first MOS transistor in the first well.~~

~~13. (Previously Added) The semiconductor device as claimed in claim 1, further comprising:~~

~~a second well having a first conductivity type formed in a second region of the semiconductor substrate, wherein the heavily doped region of buried layer having a second conductivity type is not formed at an interface between the first and second wells.~~

~~14. (Previously Added) The semiconductor device as claimed in claim 1, further comprising:~~

~~a second well having a first conductivity type formed in a second region of the semiconductor substrate; and~~

~~a heavily doped region of buried layer having a first conductivity type not formed at an interface between the first and second wells.~~

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15. (Currently Amended) A semiconductor device, comprising:

- a semiconductor substrate;
- a first well having a second conductivity type formed in a first region of the semiconductor substrate;
- a second well having a first conductivity type formed in a second region of the semiconductor substrate; and
- a heavily doped region of buried layer having a second conductivity type not formed at an interface between the first and second wells, wherein the buried layer is within the semiconductor substrate separated from any surfaces of the semiconductor substrate.

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16. (Previously Added) The semiconductor device as claimed in claim 15, wherein the semiconductor substrate has a first conductivity type and the first and second wells are formed in a major surface of the semiconductor substrate.

17. (Previously Added) The semiconductor device as claimed in claim 15, further comprising:

- a heavily doped region of buried layer having a first conductivity type not formed at an interface between the first and second wells.

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18. (Previously Added) The semiconductor device as claimed in claim 17, wherein the concentration of the heavily doped region of buried layer having the first conductivity type is higher than that of the second well and lower than that of the second contact region.

19. (Previously Added) The semiconductor device as claimed in claim 17, wherein the concentration of the heavily doped region of buried layer having the second conductivity type is higher than that of the first well and lower than that of the first contact region.

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20. (Currently Amended) The semiconductor device as claimed in claim 15, wherein the heavily doped region of the first second conductivity type ~~does not extend under~~ a second MOS transistor in the second well is separated from a first contact region.

21. (Currently Amended) The semiconductor device as claimed in claim 15, further comprising a first MOS transistor having the first conductivity type and a first contact region having the second conductivity type formed in the first well, wherein the heavily doped region of buried layer having a second conductivity type is formed between the first contact region in the first well and an interface between outer surface of the first well and within the semiconductor substrate ,and wherein the heavily doped region is separated from the first contact region.

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22. (Currently Amended) The semiconductor device as claimed in claim 21, further comprising:

a second MOS transistor having the second conductivity type and a second contact region having the second conductivity type formed in the second well; and

a heavily doped region of buried layer having the first conductivity type formed between the second contact region in the second well and an interface between outer surface of the second well and within the semiconductor substrate.

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23. (Previously Added) The semiconductor device as claimed in claim 15, wherein the heavily doped region of the second conductivity type does not extend under a first MOS transistor in the first well.

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24. (Currently Amended) A semiconductor device comprising:
a semiconductor substrate having a first conductivity type;
a first well having a second conductivity type formed in a first region in a major surface of the semiconductor substrate;
a first MOS transistor having the first conductivity type and a first contact region having the second conductivity type formed in the first well;
a second well having the first conductivity type formed in a second region in the major surface of the semiconductor substrate;

Sub D > a second MOS transistor having the second conductivity type and a second contact region having the second conductivity type formed in the second well;

09 a heavily doped region of buried layer having the second conductivity type formed between the first contact region in the first well and an interface between outer surface of first well and within the semiconductor substrate and not formed at an interface between the first and second wells; and

a heavily doped region of buried layer having the first conductivity type formed between the second contact region in the second well and an interface between an outer surface of the second well and within the semiconductor substrate.

25. (Currently Amended) The semiconductor device as claimed in claim 22, wherein the heavily doped region of buried layer having a first conductivity type is not formed at an interface between the first and second wells in contact with the first or second contact regions.

Please add new claims 26-31 as follows:

Sub D > 26. (New) The semiconductor device as claimed in claim 1, wherein the heavily doped region of buried layer is located within the first well below the first contact region.

010 27. (New) The semiconductor device as claimed in claim 1, wherein the heavily doped region of buried layer prevents latch-up.

Sub D. 28. (New) The semiconductor device as claimed in claim 15, wherein the heavily doped region of buried layer is located within the first well below a first contact region in the first well.

29. (New) The semiconductor device as claimed in claim 15, wherein the heavily doped region of buried layer prevents latch-up.

30. (New) The semiconductor device as claimed in claim 24, wherein each of the buried layers are separated from each of the contact regions.

31. (New) The semiconductor device as claimed in claim 24, wherein the heavily doped region of buried layer prevents latch-up.